# Lab 3: Digital Logic Lab

Introduction

This lab involves using hardware stations provided to students at Harvey Mudd College. You will not be able to perform the tasks without access to similar hardware.

Each station is equipped with a PB-503 proto-board with 5V power supply, clock signal of variable rate, logic switches and eight LEDs. You will build all circuits on the proto-board. Several oscilloscopes are available in the lab to be shared by the stations. Also available are the various IC logic chips, which are described in Part 1 of the lab and used for the circuit designed for Part 2. A DC motor is provided at each station to be used in Part 2.

Background: Basic Logic Gates

Various logic gates, such as NOT (inverter), AND and OR, can be realized by different technologies. Here, we only consider one technology using Metal-oxide semiconductor (MOS) field-effect transistors (FET). There are two types of MOS transistors, the n-channel and p-channel, as shown in Figure 1. MOS transistors are voltage-driven, i.e., whether there is current from drain to source of the transistor (conducting or cut-off) depends on the voltage applied to its gate (with little current drawn from the input).
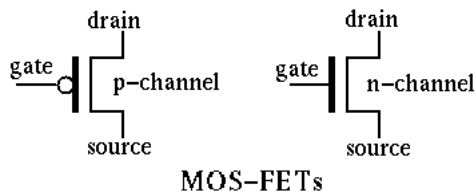
gate voltage	n-channel	p-channel
High	conducting	cut-off
Low	cut-off	conducting

FIGURE 1   P- and n-channel MOS transistors.

Various logic operations can be realized by the combination of both p-channel and n-channel MOS transistors (hence, the term complementary metal-oxide semiconductor or CMOS). For example, a NOT gate can be realized as shown in Figure 2
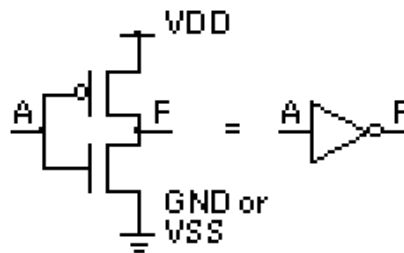

FIGURE 2   MOS NOT gate.

Verify that this is indeed a NOT gate (that is, the output voltage F is always the opposite of the input voltage A). Fill out input-output tables for each of the two CMOS circuits in Figure 3 (as always, use logical 1 and 0 to represent high and low voltage, respectively), and determine the logical relationship between the output and the two inputs.
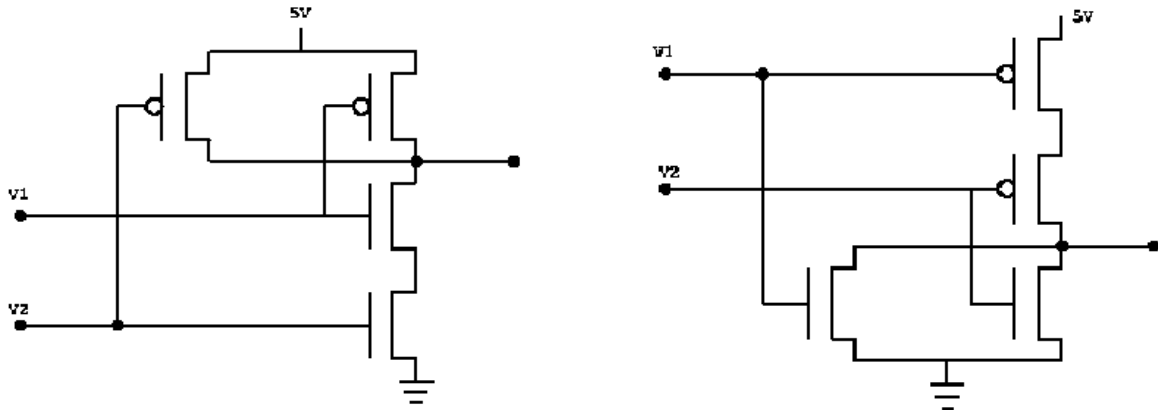
FIGURE 3   Two CMOS circuits.

Part 1: Basic Logic Circuits

This lab uses the 7400 family of TTL logic IC chips. Carry out the tasks specified in each of the items below. They will prepare you for the design and construction of the circuit needed for the second part of the lab.

NAND gates (7400)

An input of 5V is a logical 1 and 0V (ground) is logical 0 (i.e., positive logic). Verify the truth table for one of the NAND gates. What logical value is an open input terminal treated as by the circuit? Construct an AND gate from two NANDs. Verify the truth table. Construct an OR gate from NAND gates. How many NANDs do you need? Verify the truth table.
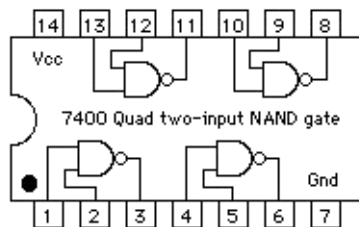

FIGURE 4   NAND gates (7400).

Set-Reset Flip-Flop (RS-FF)

Build an RS latch with two NAND gates, as discussed in Appendix B of *Computer Organization and Design* (included with this CD). Verify the truth table of the RS latch. Then add two more NAND gates to build an RS-FF with *S*, *R* and *Clock* inputs. Verify the truth table.

Delay Flip-Flop (D-FF) (74LS74)

The IC chip 74LS74 has two D-FF's. Each D-FF has a D input as well as the clock. In addition, two asynchronous inputs $\overline{CLEAR}$ and $\overline{PRESET}$, when they are 0, can set the D-FF to 0 and 1, respectively. These operations are independent of the clock; therefore, the name asynchronous. When you don't want to preset or clear, they should not be grounded. Verify the truth table for a D-FF, excluding the clear and preset. What value is an open input treated as? On what edge of the clock do the outputs change?

Describe how you could use a D-FF to determine the direction of rotation of the motor shaft described in Part 2.
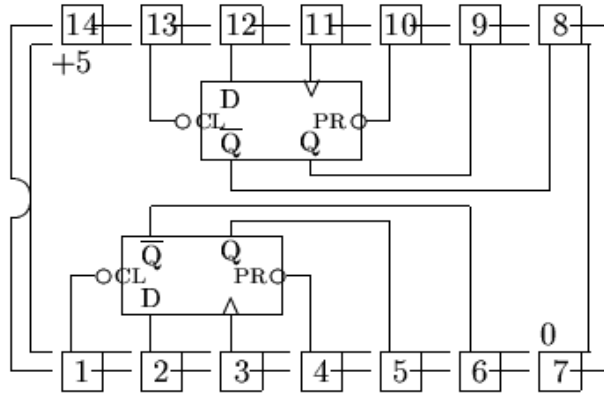
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FIGURE 5   Delay Flip-Flops (74LS74).

Toggle Flip-Flop (T-FF)

Use a D-FF to construct a FF whose output changes state at every clock (equivalent to T=1 of a T-FF). Build a 4-bit up counter and then a down counter by four such FFs. Then build a decade counter that up counts from 0 to 9. (Hint: use the output to $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ the FFs.)

Binary Decoder (74LS139)

The IC chip 74LS139 has two binary decoders. In addition to Vcc and Ground, each decoder has two inputs A and B, and 4 outputs Y0, Y1, Y2 and Y3. Moreover, an $\overline{\text{ENABLE}}$ input is used so that the circuit will function only when $\overline{\text{ENABLE}} = 0$. Find out the truth table of the decoder. If B=0, which of the output is identical to A? If B=1, which output is identical to A?
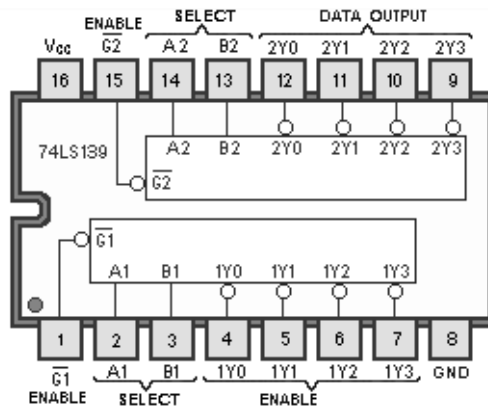

FIGURE 6   Binary Decoder (74LS139).

4-Bit Up/Down Counters (74LS193)

This counter will up-count the pulses sent to COUNT_UP while COUNT_DOWN=1 and down count the pulses sent to COUNT_DOWN while COUNT_UP=1. The counter can be cleared by CLEAR=1 so that all four outputs. O_A, O_B, O_C, and O_D, are reset to 0. When LOAD=0, the counter will be set to a value specified by the four inputs, DATA_A, DATA_B, DATA_C and DATA_D.

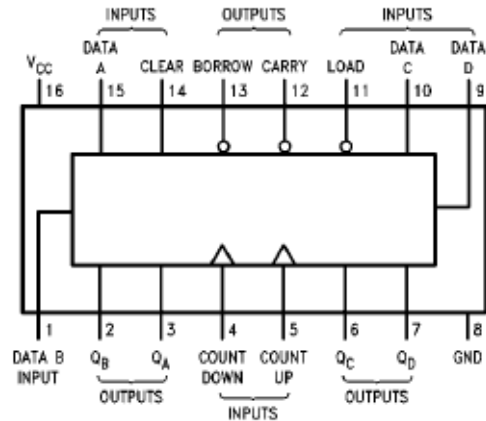Connect the counter to count from 3 to 11.

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FIGURE 7   Up/Down counter (74LS193).

Several such counters can be cascaded to form 8-bit, 12-bit and 16-bit up/down counters by connecting the CARRY and BORROW outputs of one counter to, respectively, the COUNT_UP and COUNT_DOWN inputs of the next counter.

Part 2: The Design

Design a circuit to monitor the angular position of a link attached to a DC motor with an optical encoder. Inside the encoder are an infrared source and two sensors. As the motor turns, a set of slits pass between the source and each sensor, which produces a 5V square wave. There are 1000 slits in one revolution of the encoder. The signals produced by the two sensors (green and yellow wires) are identical but 90 degrees out of phase with each other. A motor turning at a constant speed would produce the signals shown in Figure 8. Also, there is a gear box attached to the motor shaft with a reduction ratio of 1:48, so that one revolution of the link corresponds to 48,000 pulses in the output signals.
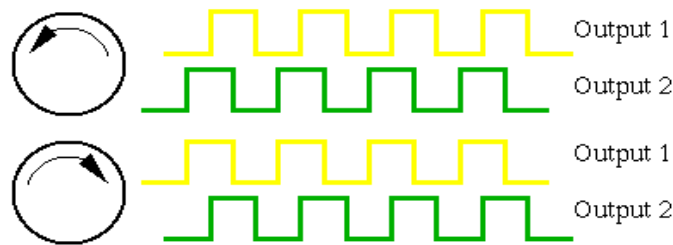

FIGURE 8   Motor rotation encoder signals.

A 5V power supply (red wire for 5V and black for ground) is needed by the motor as well as the TTL chips inside. *Important: Do not use a power supply higher than 5V!* Otherwise the TTL chips will be damaged.

Taking the two signals from the encoder of the motor as the inputs, your circuit should determine the direction and angle of rotation, by up- or down-counting the pulses of the output of the motor. The outputs of the counters are displayed by the LEDs on the proto-board.

- Check the operation of the encoder by observing the outputs of the encoder of the motor while manually rotating the motor.

- Determine the number of bits required to monitor the position of the link attached to the gear box for a range of –90 to 90 degrees from the vertical position.

- Determine the direction of the motor rotation with the D-FF so that clockwise and counter clockwise rota-

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tions are represented by logic `1` (or `0`) and `0` (or `1`), respectively.

- Based on the direction, build the circuit to generate the count-up and count-down signals needed to drive the 74LS193 up-down counters.

- Connect enough counters to tally the pulses from the outputs of the motor. Display the highest eight bits on the LEDs. Determine the resolution of the display in terms of the smallest angle increment measurable.

- Use the CLEAR or LOAD inputs to pre-set the counter when the link is vertical. Tabulate the binary values corresponding to the link angles of –90, –45, 0, 45 and 90 degrees. Compare the expected values with the actual displayed by the LEDs.

- Draw a full schematic of your logic circuit showing all connections of the components (74LS*xxx*) used in the design.