Computer Architecture COM 3200

Course Description:

The word "architecture" has different meanings in different areas of computer science. For the purpose of this course, it is where the software meets the hardware. Hence, in a layered model, this is the study of a layer that lies just below the operating system, and yet above the layer of circuit layout. This subject has always been important to computer scientists in order to achieve the full performance of the architecture. As current VLSI technology approaches some fundamental physical limits on speed and size, one can foresee large departures from traditional architectural models in the future. This makes the issue of computer architecture ever more pressing for demanding applications.

The first part of this course will concentrate on issues affecting a typical desktop PC and will largely follow the textbook. The second part of this course will concentrate on issues affecting a multiprocessor server, including an implementation of SMP (Synchronous MultiProcessor) The second part of the course will include a mini-project with significant threads programming.

Faculty Information:

Professor G. Cooperman Office: 215 Cullinane Hall e-mail: gene@ccs.neu.edu Phone: (617) 373-8686 Office Hours: Thurs. at 4:45, Thurs. at 8:30 and by appointment.

Textbook: Computer Systems Design and Architecture, V.P. Heuring and H.F. Jordan, Addison-Wesley, 1997

Exams and Grades:

There will be three to four homework assignments over the quarter, plus a midterm and a final. They will be weighted 40% for the final, 30% for the midterm, and 30% for the homework. All homework assignments will be equally weighted.

Syllabus:

Week	Topics	Chapter
Jan. 2	Introduction and Memory Subsystem	Class Lecture
Jan. 9	Instruction Set Architectures, RTN notation	Ch. 2 and 3, App. B and C
Jan. 16	Processor Design	Ch. 4.0–4.5
Jan. 23	Advanced Processor Design, Pipelining	Chap. 4.6–4.8, 5.1, App. A
Jan. 30	Instruction-Level Parallelism (ILP) & Microprog	Chap. 5.2–5.3
Feb. 6	Memory components revisited and Cache	Ch. 7.1–7.5
Feb. 13	Mid-term, followed by Virtual Memory	7.6 - 7.7
Feb. 20	I/O and Peripherals	Ch. 8 and 9
Feb. 27	POSIX threads and SMP	(Handouts)
Feb. 28	SMP: Cache coherence	(Handouts)
Mar. 6	Memory consistency and DSM	(Handouts)
Mar. 13	Final Exam	